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Replacement of SF_6 with N_2/CO_2 in design of a parallel-fed voltage multiplier for electrostatic accelerator

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H I G H L I G H T S

- Design of a 500 kV/15 kW electrostatic high-voltage generator is presented.
- Modifications in high-voltage structure make using lower insulating N_2/CO_2 instead of SF_6 possible.
- The modified structure is capable of generating 500 kV with N_2/CO_2 and 1.1 MV with SF_6.

A B S T R A C T

Two main insulating gases of SF_6 and N_2/CO_2 mixture are employed to increase voltage capability of electrostatic accelerators. SF_6 offers more insulating capability, but environmental and technical disadvantages of SF_6 makes usage of N_2/CO_2 mixture a desirable option. This paper aims to replace SF_6 with N_2/CO_2 in design of a 500 kV/30 mA parallel-fed voltage multiplier. High-voltage section of the accelerator is a capacitive structure which in combination with rectifying elements, generates the accelerating high-voltage. The structure which is called Voltage Multiplier Capacitive Structure (VMCS) is designed and analyzed in this paper. The first structure is designed to employ SF_6 as insulating gas (VMCS500). Then, the structure is modified to be capable of using N_2/CO_2 as insulating gas with lower breakdown voltage (VMCS500-m). The modified structure requires more complex mechanical manufacturing process, but offers the simplicity of using N_2/CO_2 mixture, the option of using the modified structure with superior SF_6 gas, increasing the output voltage and beam energy. CST EM STUDIO was used for capacitance calculation and electric field analysis. LTSPICE was used for equivalent circuit analysis of the high voltage generating section.

K E Y W O R D S
Accelerator
Electrostatic
High-voltage
Cascade generator
Insulating gas

H I S T O R Y
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1 Introduction

Electrostatic accelerators, which constitute a major fraction of the world's industrial accelerators, have two main sections; high-voltage generator and particle accelerating tube. Two main types of high-voltage generators are Van-de-Graaff generators and high-voltage-multiplier generators (Hellborg, 2005). Cockcroft-Walton is the most basic type of multiplier-based high-voltage generators, which is also known as cascade generator (Hellborg, 2005; Scharf and Scharf, 1991).

After design and manufacturing of a 200 keV electrostatic accelerator in Nuclear Science and Technology Research Institute of Iran, NSTRI (Rahighi et al., 2013), design of an electrostatic accelerator with particle energy up to 500 keV and ability to supply currents up to 30 mA was targeted. Inductive and capacitive coupled parallel-fed cascade generators are two ways which have their advantages and are used in different accelerators. Capacitive coupled cascade generators are reported to be used in ion and electron applications (Nayak et al., 2016; Brand, 1989).

In capacitive coupled generators, input alternating voltage in the range of a few kHz to hundreds of kHz are fed to a multi-stage capacitive structure. The rectified voltage of each stage add up and produce the output accelerating DC high-voltage (Cleland and Morganstern, 1960). The capacitive structure is formed by semi-cylindrical

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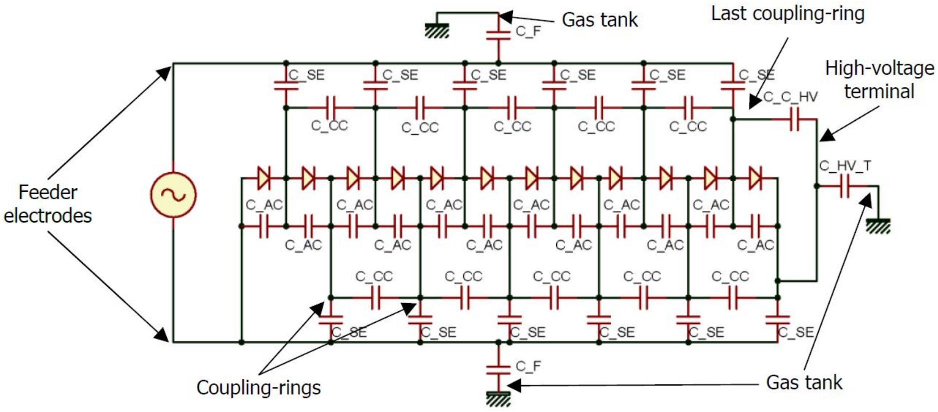

Figure 1: A parallel-fed capacitive coupled cascade voltage multiplier circuit (Nazari et al., 2020).

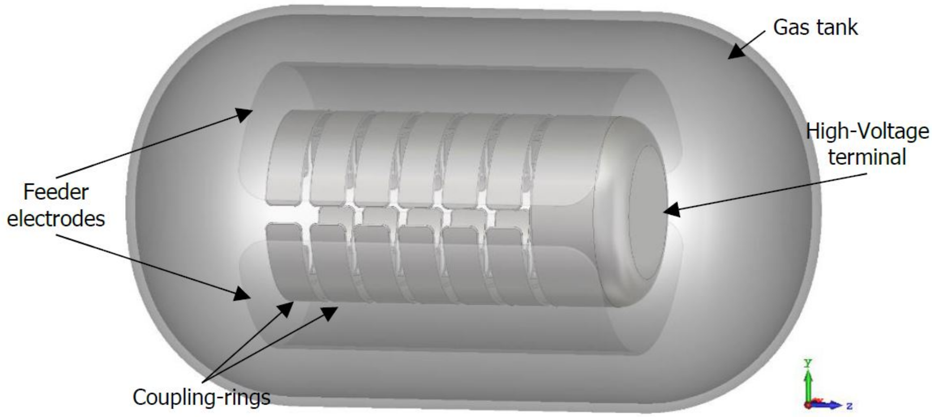

Figure 2: A voltage multiplier capacitive structure (VMCS) of a parallel-fed capacitive coupled voltage multiplier.

electrodes that are put into a gas-filled tank along with rectifying units. The gas-filled tank elevates high-voltage safety of the device. The equivalent circuit of the structure includes series of unintended capacitors, which is being shown in Fig. 1 (Nazari et al., 2020).

As shown in Fig. 2, the voltage multiplier capacitive structure (VMCS) is a series of electrodes which constitute capacitive elements of a voltage multiplier. The desired voltage-current output of the voltage multiplier is presented in Table 1.

Table 1: Desired specifications of the VMCS.

Parameters	Value
Input voltage amplitude	50 kV
Input frequency	100 kHz
Output voltage	500 kV
Maximum load power	15 kW
Output voltage ripple	$\leq 5\%$

Equations (1) to (4) describe the overall behavior of an ideal VMCS circuit. Output voltage, V_{out}, is a function of n, V_0, V_{drop}, V_{ripple} and k which are number of stages, amplitude of input voltage, voltage drop and voltage ripple in presence of load, and coupling factor respectively. I is the load current, C_{se} and C_{ac} are coupling capacitance and shunt capacitance of a typical stage and f is the frequency of the input voltage (Cleland and Farrell, 1965; Thompson and Cleland, 1969). Frequency, input voltage amplitude, number of stages and capacitance values are important parameters affecting voltage-current output of the voltage multiplier. Shape, dimensions and distance of electrodes and insulating gas withstand capability determine achievable capacitance values of the voltage multiplier.

$$V_{out} = \frac{nV_0}{k} - V_{drop} \pm V_{ripple} \tag{1}$$

$$k = 1 + \frac{4C_{ac}}{C_{se}} \tag{2}$$

$$V_{drop} = \frac{I(n-1)}{f\,C_{se}\,k} \tag{3}$$

$$V_{ripple} = \frac{I}{2f\,C_{se}} \tag{4}$$

This article presents two different design of a high-power voltage multiplier for an electrostatic accelerator. The first design is based on SF_6 as insulating gas and presents mechanically simpler structure and the second design tries to eliminate the need to SF_6 greenhouse gas and modifies the structure to achieve the same voltage-current output with N_2/CO_2 mixture as insulating gas.

Figure 3: A proof-of-concept model of a parallel-fed capacitive coupled voltage multiplier.

2 Materials and methods

Design of the VMCS was carried out in a loop with three steps:

1. Capacitance calculation
2. Equivalent circuit simulation
3. Voltage gradient withstand analysis

Each point with excess electric field will be redesigned and steps (1) to (3) will be processed for the new design. These steps will be described in following sections. The design process was started with following assumptions: rectifying-stacks' specifications and insulating gas properties.

2.1 Rectifying-stacks and Insulating Gas Specifications

The rectifying elements of each stage play the role of converting input alternative high-voltage to a high-voltage DC output, and in high-voltage applications they are created by series of diodes to withstand higher voltage and current levels (Galloway et al., 2004; Hellborg, 2005). Rectifying-stack is a series of solid-state diodes, paralleled with subtle-fabricated protective spark-gaps (Ghodke et al., 2013).

The main part of the shunt capacitance in Fig. 1 (C_{ac}) is the overall capacitance of the rectifying-stack which is the overall capacitance of protective spark-gap, cladding and diodes junction capacitance. Ability to sustain input voltages up to two times of the input high frequency voltage, minimum value of overall capacitance and ability to withstand higher average currents are desired characteristics of rectifying-stacks. Based on available HV diodes, rectifying-stacks are assumed to have less than 3pF of capacitance, more than 50kV working repetitive peak reverse voltage, more than 500mA forward current sustainability of and less than 30 cm of length.

SF_6 and N_2/CO_2 are among the most commonly-used insulating gasses. SF_6 and N_2/CO_2 (80%/20%) are reported to have 25 MV.m^{-1} and 9.6 MV.m^{-1} (at 14 atm) direct high-voltage withstand capability, respectively (Cottereau, 2001).

SF_6 offers greater insulation but due to its expensiveness (Hellborg, 1996), sensitivity to gas impurity (LG Christophorou, 2004), toxic breakdown byproducts (Hellborg, 2005) and high GWP2 index (LG Christophorou, 2004), it necessitates deployment of special gas-handling system (LG Christophorou, 2004). There is a trend toward alternatives of SF_6 in high voltage applications (LG Christophorou, 2004). N_2/CO_2 mixture, as an alternative, offers less insulation, but cost-efficiency, chemical inactivity and environmental acceptance are its advantages (LG Christophorou, 2004).

2.2 Design of the Voltage Multiplier Capacitive Structure (VMCS)

Capacitance calculation, circuit analysis and high-voltage withstand analysis are the three steps of designing the VMCS.

CST EM STUDIO was chosen to calculate capacitance values and high-voltage withstand analysis. It was cross-checked with theoretical equation for electric-field and capacitance calculations. Results had less than 0.4% error for capacitance calculation and less than 2% error for electric-field calculation. Figure 3 shows a prototype capacitive structure which was constructed to benchmark results and to prove the concept of the parallel-fed capacitive coupled voltage multiplier. Experimental measurements have shown less than 10% deviations from calculated capacitance values.

LTSPICE was chosen to study equivalent circuit of the VMCS. It was chosen for its ability to accept text-based schematic file as its input. An AutoIt code was developed to transfer circuital analysis data from/to CST STUDIO SUIT (Hasanpour, 2021). The developed code generates VMCS circuit schematic input file for LTSPICE with the extracted capacitive values from CST EM STUDIO result.

The last stages coupling rings and HV terminal have with highest surface electric fields, so electric-field levels in these points and insulting gas properties defines the radial configuration of the VMCS. The radial configuration leads to estimated values of created capacitive elements. Number of stages will be calculated using Eqs. (1) to (4) by having input voltage, desired beam energy and current, rectifying- stacks overall specifications. Edges and tips of electrodes are place with highest electric field so shapes, distances and sharpness of these points are designed carefully.

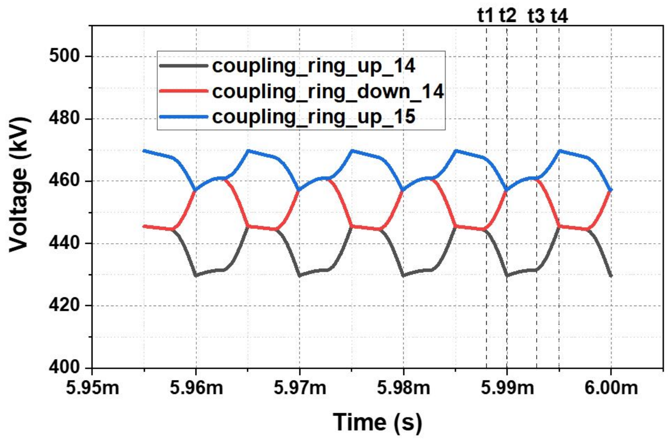

Figure 4: Electric potential variation in coupling rings of last two stages and selected time-points of high-voltage withstand analysis.

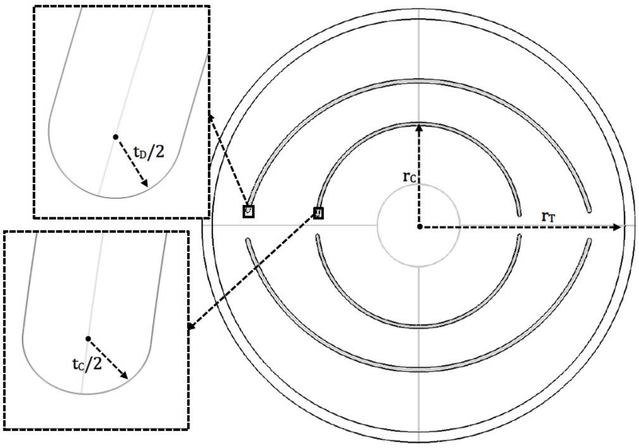

Figure 5: Normal-to-column prospect of VMCS500 (SF_6-based design).

Table 2: Geometrical properties of VMCS500 (SF_6-based design).

Parameter	Unit	Values
r_C	mm	250
r_D		425
r_T		500
d_D		160
I_D		2160
I_C		100
I_H		250
g_c		20
r_{Dt}		140
r_{Ct}		20
r_H		110
t_D		10
t_C		8
t_H		8
a_C	$\pi/180$ rad	10
a_D		30
n	#	15

Every node of the voltage multiplier circuit carries a time-variable voltage. Voltage on each plate is extracted from circuit analysis, as in reality, so capacitance calculation and circuit analysis must be done before electric field analysis. As these variable voltages create variable electric fields on each electrode, high-voltage withstand analysis should be done in different phases of voltage. Figure 5 shows how voltages on last three coupling rings vary over time and specifies 4 critical time-points.

According to Fig. 4, there are extreme situations for the last two stages coupling rings; $t1$ is the time which the connecting diode stack is in forward mode, so these two electrodes are equipotential and $t2$ which the diode stack is in reverse mode where they are under their maximum potential difference, $t3$ and $t4$ are time-points where extreme situations happen between two coupling rings of consecutive stages. Electric fields in these 4 critical time-points are analyzed separately to ensure stability of the structure under time-variable high-voltage.

As insulating gas properties sets limit to maximum permissible electric field inside the structure, it affects final geometry. In the first attempt, SF_6 was considered as insulating gas and a 50 kV/100 kHz alternating voltage as input and a valid design of the VMCS was presented (VMCS500). Then N_2/CO_2 mixture was assumed as insulating gas and the geometry was modified to make it compatible with N_2/CO_2 insulation level and achieved another acceptable design for the VMCS (VMCS500-m). Among the important parameters described in Sec. 1, frequency, amplitude of input voltage and number of stages are kept fix in 100 kHz, 50 kV and 15, respectively. Insulating gas pressure which is effective in insulation level are considered the same in both cases (14 atm). Designed geometries, the resulting equivalent circuit and high-voltage withstand analysis of the structures are presented in Resultssection.

3 Results

3.1 Geometry

3.1.1 SF_6-based Design (VMCS500)

Dimensions presented in Fig. 6 and Table 2 which are resulted from design loop, create sufficient capacitive elements to achieve 500 keV output with 15 kW load power and have acceptable maximum surface electric-field.

Coupling rings and feeder electrodes have semi-cylindrical geometries and HV terminal is closed-base cylinder. Coupling rings are placed in a coaxial arrangement and have the same radius of the HV terminal. This arrangement created higher capacitive element between feeder electrodes and coupling-rings and also kept edges of the electrodes the farthest possible. Figure 5 shows a normal-to-column prospect of SF_6-based design (VMCS500).

Feeder electrode surrounds the HV terminal as well as the coupling-rings' column. This arrangement reduces observed electric-field on feeder electrodes heading edge. Alignment of the coupling-rings and the HV terminal is important and should be considered in construction phase. Choosing the same radius for the HV terminal and

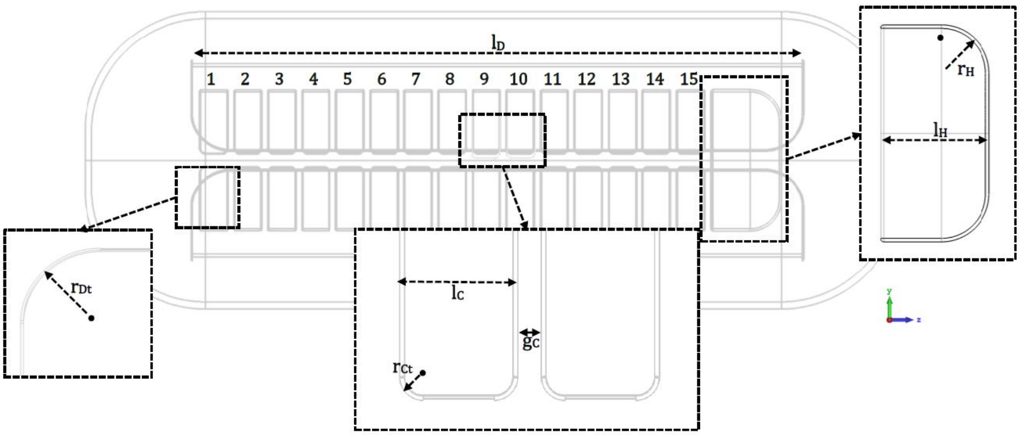

Figure 6: Parallel-to-column prospect of VMCS500 (SF_6-based design).

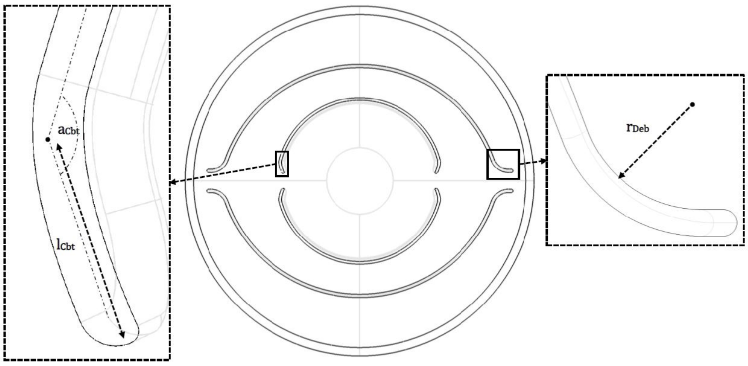

Figure 7: Normal-to-column prospect of VMCS500-m (N_2/CO_2-based design).

coupling-rings helps reducing observed electric-field on the heading edges of the last coupling-ring. The fact that the last coupling rings and feeder electrodes have the highest potential difference leads to creation of a high electric field on the mentioned electrodes, so edges of these electrodes have been blended to reduce created electric-field. Figure 6 shows a parallel-to-column prospect of VMCS500.

Geometrical values of the SF_6-based design of the VMCS is presented in Table 2. Edges and tips in all components are blended to the highest possible radius (Fig. 5).

3.1.2 N_2/CO_2-based Design (VMCS500-m)

VMCS500-m (N_2/CO_2-suitable design) which is presented in Figs. 7 and 8 is not constituted by ordinary cylindrical shaped electrodes. Arrangement and sizes of components are the same as VMCS500 but edges and tips of electrodes where excessive surface electric-field are re-designed. A normal-to-column view (Fig. 7) shows new subtle-designed edges of feeder electrode and coupling-rings. Bending coupling-rings' edges inward and feeder electrodes' edges outward, reduces surface electric-field on both groups of electrodes.

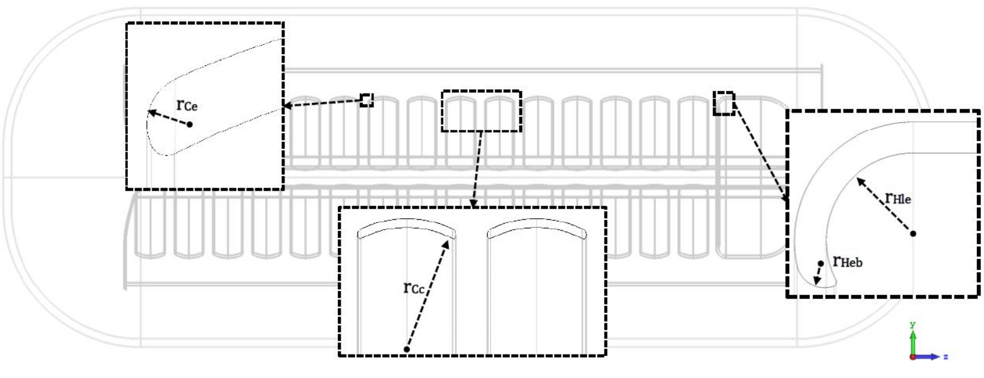

Figure 8: Parallel-to-column prospect of VMCS500-m (N_2/CO_2-based design).

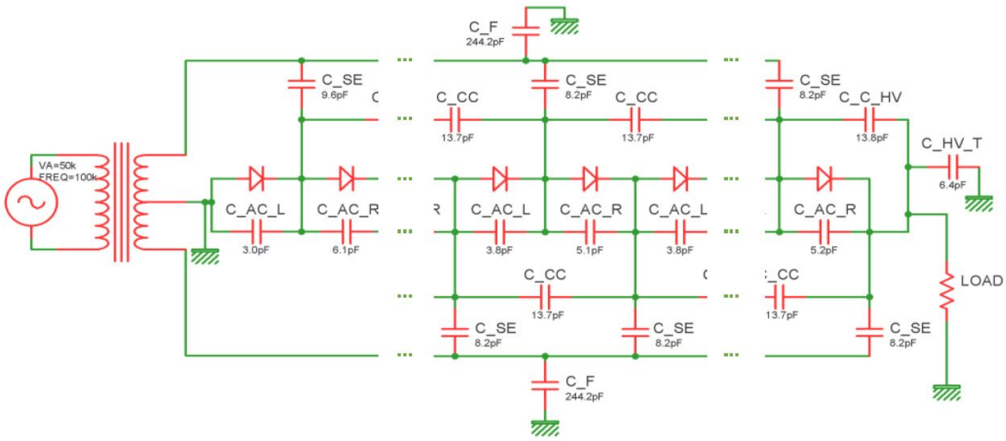

Figure 9: Equivalent circuit of VMCS500 and VMCS500-m.

Parallel-to-column modifications to the geometry include designing curved surface coupling-rings, bent bottom edge of HV terminal and asymmetrically blended edges which are being shown in Fig. 8. New design of the coupling-rings and HV terminal and asymmetrically blended edges play the main role in elimination of coupling-rings-edges to feeder-electrode-surface electric-field components of the surface electric-field. Parallel-to-column view of VMCS500-m (N_2/CO_2-based design) and detailed information of the geometry properties are presented in Fig. 8 and Table 3.

Table 3: Geometrical properties of VMCS500-m (N_2/CO_2-based design).

Parameter	Unit	Values
r_{Deb}		50
r_{Cbt}		30
r_{Cc}	mm	100
r_{Hle}		30
r_{Heb}		7
r_{Ce}		6
a_{Cbt}	$\pi/180$ rad	40

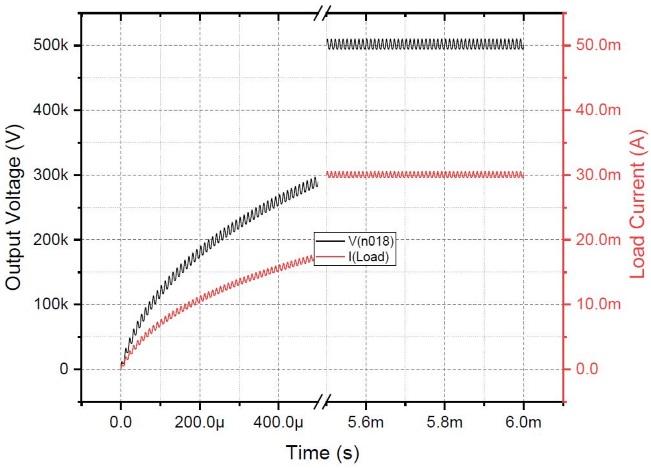

Figure 10: Output voltage-current of the designed voltage multiplier.

3.2 Voltage-Current Output (VMCS500 and VMCS500-m)

The described structure constitutes the capacitive elements of a parallel-fed voltage multiplier circuit. Capacitive elements were calculated by CST EM STUDIO. Equivalent circuit of the voltage multiplier is presented in Fig. 9. Capacitive values of C_{se}, C_{ac-r}, C_{ac-l}, C_f, and C_{cc},

Voltage-current output of the voltage multiplier is presented in Fig. 10. The designed structure with assumed rectifying-stacks' characteristics results in a 3.2% ripple in voltage in 500 kV accelerating voltage and 30 mA of load current.

Capacitive elements formed in both structures were not affected by slight geometrical modifications, so voltage and current outputs were identical in both designs (VMCS500 and VMCS500-m).

3.3 High-Voltage Withstand Analysis

3.3.1 SF_6-based Design (VMCS500) HV Analysis

As explained in Sec. 2.2, inspection of surface electric-field was done in four critical time points on all electrodes. As CST EM SUDIO uses tetrahedral mesh method to analyze the given model, sizes of mesh cells are usually reported by their "edge size". In our research we employed "Adaptive Mesh Refinement" method which in addition to focusing on edges, preforms an iteration of mesh improvement to achieve minimize calculation error. "Min. edge length" of 0.574073 mm has been achieved for VMCS500 CST EM SUDIO solver. Surface electric-fields were calculated with total number of 10.4 M tetrahedral mesh cells with localized meshing focused on coupling-rings. The maximum surface electric-field of the structure is presented in Table 4.

Maximum surface electric-field never exceeds 14 $MV.m^{-1}$ on any electrode. Maximum surface electric-field is on coupling-ring #14. Parallel-to-column and Normal-to-column sectional view of electric-field magnitude inside the structure is shown in Fig. 11 and Fig. 12.

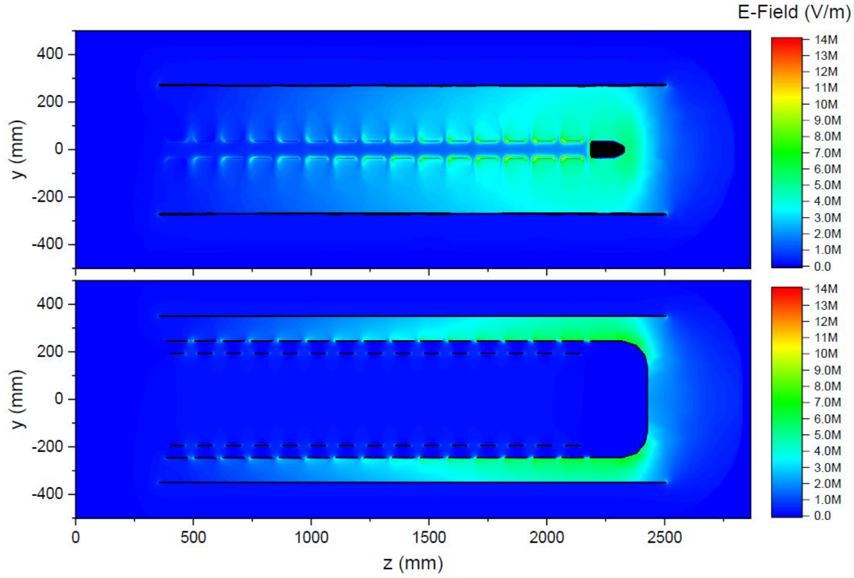

Figure 11: Cross-sectional view of electric-field magnitude in VMCS500 (SF_6-based design), down: at $x = 0$ (symmetry plane), up: at $x = 247$ (edges of coupling-rings' column).

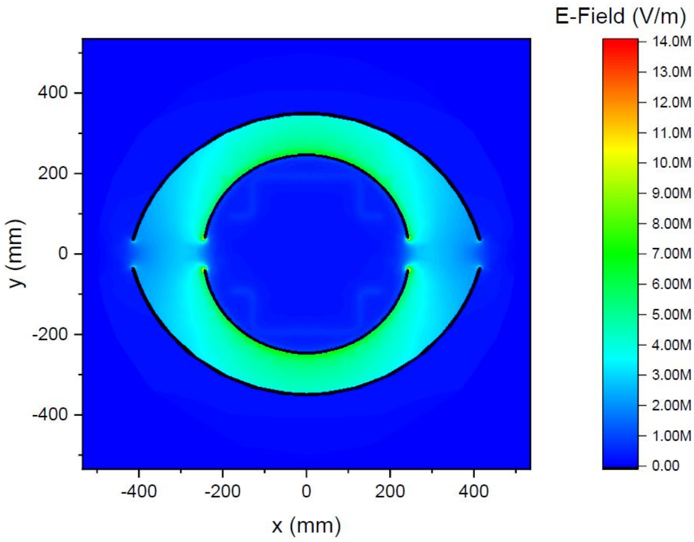

Figure 12: Normal-to-column view of electric-field magnitude in VMCS500 (SF_6-based design)on semi-last coupling-ring ($z = 1947$).

Table 4: Maximum surface electric-field in VMCS500 (SF_6-based design).

Electrode Name	Max E-field ($MV.m^{-1}$)
Feeder electrodes	6.80
HV terminal	10.20
coupling-ring up #14	12.67
coupling-ring up #15	13.33
coupling-ring down #14	13.96
coupling-ring down #15	13.49

As presented, the modified structure described in Fig. 5, Fig. 6 and Table 2 is capable of generating 500 kV of output voltage with the same input voltage. As insulating level of SF_6 is more than 14 $MV.m^{-1}$, this structure (VMCS500) is capable of production of voltages higher than 500 kV with higher input voltage amplitude.

3.3.2 N_2/CO_2-based Design (VMCS500-m) HV Analysis

The new design of feeder electrodes and coupling-rings' column has increased time-average of maximum surface electric-field on feeder electrode by 3% but decreased coupling-rings column and HV terminal by 37% and 9%, respectively, enabling the whole structure to work within insulation range of N_2/CO_2 mixture. Surface electric-fields were calculated by CST EM SUDIO with total number of 10.1 M tetrahedral mesh cells, "Min. edge length" of 0.49870 mm and localized mesh setting. The maximum observed surface electric-field of the N_2/CO_2-based VMCS (VMCS500-m) are presented in Table 5.

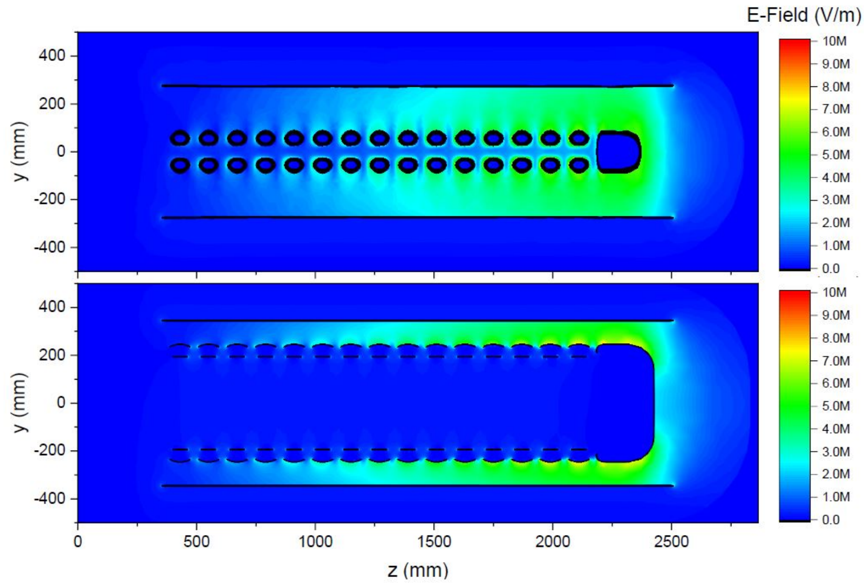

Figure 13: Cross-sectional view of electric-field magnitude in VMCS500-m (N_2/CO_2-based design), down: at $x = 0$ (symmetry plane), up: at $x = 232$ (edges of coupling-rings' column).

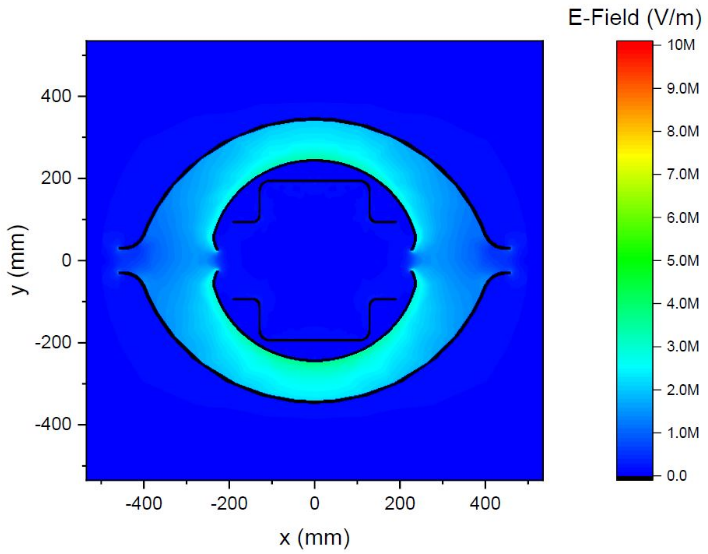

Figure 14: Normal-to-column view of electric-field magnitude in VMCS500-m (N_2/CO_2-based design) on last coupling-ring ($z = 2089$).

Table 5: Maximum surface electric-field in VMCS500-m (N_2/CO_2-based design).

Electrode Name	Max E-field ($MV.m^{-1}$)
Feeder electrodes	6.43
HV terminal	9.23
coupling-ring up #14	8.62
coupling-ring up #15	8.89
coupling-ring down #14	8.74
coupling-ring down #15	8.64

Maximum surface electric-field inside the model is observed on HV terminal and it never exceeds 9.23 $MV.m^{-1}$ on any electrode. Parallel-to-column and Normal-to-column sectional view of electric-field magnitude inside the N_2/CO_2-based structure (VMCS500-m) is shown in Figs. 13 and 14.

As described, substituting SF_6 with N_2/CO_2 is possible with the redesigned structure presented in Fig. 7, Fig. 8 and Table 3. As there were no significant change in capacitive values, voltage-current output of the N_2/CO_2-based design are identical to SF_6-based design (500 kV, 30 mA). This geometry (VMCS500-m) is capable of achieving output voltages up to 1.1 MV with higher input voltage amplitudes and SF_6 as insulating gas.

4 Conclusions

Design and simulation of a 500 kV/15 kW parallel-fed cascade voltage multiplier for an electrostatic accelerator was done and presented in this article. Replacing SF_6 with N_2/CO_2 mixture was considered as an approach and two different design were performed.

CST EM STUDIO and LTSPICE are suitable codes for calculation of capacitance, electric-field, and circuit analysis in design and simulation of a voltage multiplier. CST EM STUDIO results showed less than 10% deviations from experimental measurements of capacitance values on a proof-of-concept model, and less than 1% and 2% from theoretical calculations of capacitance and electric-field values, respectively.

Interface code which was developed in this research facilitates using CST EM STUDIO and LTSPICE in simulation and analysis of voltage multiplier capacitive structure (VMCS). It can reduce human errors and facilitate analyzing effects of modification of electrodes in voltage-current output of VMCS.

Two designs were performed in this research. The first design used the superior SF_6 gas as insulating gas for generating 500 kV/15 kW VMCS (VMCS500). Then, the structure was modified to be suitable for lower insulating N_2/CO_2 mixture with the same input and output (VMCS500-m). VMCS500 has a mechanically simpler design but uses SF_6 and VMCS500-m uses N_2/CO_2 mixture and has a more difficult mechanical construction

Result of the simulation show that modifications in shapes and sizes of electrodes of the VMCS reduces magnitude of electric field on critical points up to 37%. This allows usage of N_2/CO_2 mixture, which has lower cost and environmental impact in comparison to SF_6. VMCS500-m design will be used to construct a 500 kV electrostatic accelerator in NSTRI.

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